

**Dual Hardmask Process for the formation of Copper/Low-K  
Interconnects**

ABSTRACT

The invention describes a method for forming integrated  
5 circuit interconnects using a dual hardmask dual damascene  
process. A first hardmask layer (50) and a second hardmask  
layer (60) are formed over a low k dielectric layer (40).  
The trench pattern is first defined by the second hardmask  
and via pattern is then defined by the first hardmask. Any  
10 interaction between low k dielectrics (40) and the  
photoresist (80) at patterning is prevented. The BARC and  
photoresist may be stripped before the start of the  
dielectric etching such that the low k dielectric material  
is protected by the hardmasks during resist strip.

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